AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A ball grid array package comprising:

a base IC structure, the base IC structure comprising:

a base substrate having a first base substrate face, a second base substrate face opposite to said first base substrate face, a base substrate opening extending between said first base substrate face and said second base substrate face, and a base conductor;

a first semiconductor chip, comprising a first chip face, a second chip face opposite to said first chip face, and first bond pads disposed over said base substrate opening; and

a first plurality of wires disposed to pass through said base substrate ~~base~~ opening and electrically connecting said first bond pads to said base conductor; and

a secondary IC structure, comprising:

a second substrate having a first secondary substrate base, a second secondary substrate face opposite to said first secondary substrate face, a secondary opening extending between said first secondary substrate face and said second secondary substrate face, and a secondary conductor;

a second semiconductor chip, comprising a first secondary chip face, and a second bond pad disposed over said secondary opening; and

a second plurality of wires electrically connecting said second bond pads to said secondary conductor through said secondary opening;

a first encapsulant filling said secondary opening around said second plurality of wires and covering said second secondary substrate face; and

a third plurality of wires connecting said secondary IC structure to said base IC structure;

wherein said secondary IC structure is mounted on said base IC structure;

2. (original): A ball grid array package according to claim 1, wherein:

said base substrate further comprises a plurality of vias extending between said first base substrate face and said second base substrate face;

said base conductor extends through said vias; and

said base substrate further comprises a layer of solder mask disposed on portions of said first and second chip faces.

3. Cancelled.

4. Cancelled.

5. (currently amended): The ball grid array package according to claim 1 [[4]] , further comprising molding compound encapsulating at least portions of said base IC structure and said secondary IC structure.

6. (original): The ball grid array package according to claim 5, wherein said molding compound encapsulates said third plurality of wires.

7. (original): The ball grid array package according to claim 5, wherein said first secondary chip face is free of said molding compound.

8. (currently amended): The ball grid array package according to claim 1 [[3]], further comprising:

at least one additional of said secondary IC structure mounted over said first secondary chip face; and

respective wires connecting a conductive portion of said at least one additional secondary IC structure to said base IC structure.

9. (currently amended): The ball grid array package according to claim 1 [[3]], further comprising a thermal dissipation element disposed over said first secondary chip face.

10. (currently amended): A method of assembling a ball grid array package, comprising:

providing a base IC structure, comprising a base substrate and a first semiconductor chip mounted on said base substrate in a die-down configuration;

linking ~~the~~ bond pads of ~~the~~ a base chip to the base substrate using ~~the~~ a first plurality of wires;

providing a first secondary IC structure, comprising a secondary substrate and a second semiconductor chip mounted on said second substrate in a die-down configuration;

mounting the first secondary IC structure to said base IC structure;

electrically connecting a conductive portion of said secondary IC structure to a conductive portion of said base IC structure using at least a second plurality of wires, and

encapsulating said base IC structure and said first secondary IC structure, including said first plurality of wires and said second plurality of wires.

11. (original): The method of claim 10, wherein said encapsulating step comprises first encapsulating said first secondary IC structure and subsequently encapsulating said base IC

structure and said first secondary IC structure, together with said first and second plurality of wires.

12. (currently amended): The method of claim 10, further comprising:

providing a second secondary IC structure, comprising a ~~secondary~~ third substrate and a third semiconductor chip mounted on said secondary substrate in a die-down configuration;

encapsulating said second secondary IC structure, such that encapsulant forms a substantially planar surface on the underside of said secondary IC structure;

mounting the substantially planar surface of said encapsulant to said first secondary IC structure;

electrically connecting a conductive portion of said second secondary IC structure to a conductive portion of at least one of said base IC structure and said first secondary IC structure; and

connecting the second secondary IC structure to at least one of the base IC structure and the first secondary IC structure using a plurality of wires.

13. (currently amended): The method of claim 10, further comprising encapsulating at least part of the base IC structure and the first secondary IC structure.

14. (original): The method of claim 12, further comprising encapsulating at least part of the base IC structure, the first secondary IC structure and the second secondary IC structure.

15. (original): The method of claim 14, further comprising attaching solder balls to the base IC structure.

16. (original): The method of claim 15, further comprising singulation of the entire BGA structure.

17. (original): A ball grid array package, comprising:

a base structure having a first opening;

a first IC chip on the base structure, over the first opening, the first IC chip being electrically connected through the first opening to a conductor of the base structure;

a second structure over the first IC chip, having a second opening;

a second IC chip on the second structure, over the second opening, the second IC chip being electrically connected through the second opening to a conductor of the second structure; and

an electrical connection from the base structure to the second structure.

18. (original): The ball grid array package as set forth in claim 17, further comprising an encapsulant around the first IC chip and the second structure.

19. (original): The ball grid array package as set forth in claim 18, wherein the encapsulant is also around the second IC chip.

20. (original): The ball grid array package as set forth in claim 19, wherein the encapsulant is also around the electrical connection from the base structure to the second structure.

21. (original): The ball grid array package as set forth in claim 17, wherein the first IC chip and the second IC chip are substantially the same size.